Curriculum Vitae

Shawki Areibi
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University of Guelph
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Current Position:

- Professor, School of Engineering, University of Guelph, Guelph, Ont.
- Adjunct Professor, ECE Department, University of Waterloo, Waterloo, Ont.
- Adjunct Professor, ECE Department, University of Ryerson, Toronto, Ont.

EDUCATION:

Ph.D. Electrical & Computer Engineering, University of Waterloo, **1995**
* *Advanced Combinatorial Search Techniques for Integrated VLSI Design.*
- *Design of Hybrid Algorithms using Tabu Search, Genetic Algorithms and Simulated Annealing for Circuit Layout.*

M.A.Sc. Electrical & Computer Engineering, University of Waterloo, **1991**
* *A Hardware Accelerator for Virtual-Time Distributed Simulation.*
- *Design of Special Purpose Hardware using a multiprocessor configuration.*

B.A.Sc. Computer Engineering, University of Tripoli, **1984**
* *Speech Recognition & Synthesis.*
- *Data acquisition system for sampling speech & algorithms for speech recognition.*

ACADEMIC AND PROFESSIONAL INTERESTS:

- Computer Architecture and VLSI design.
- Reconfigurable Computing.
- VLSI Physical Design Automation.
- Integrating Machine/Deep Learning into EDA CAD Tools.
- Hardware Accelerators for Machine Learning.
- Combinatorial Optimization Techniques, Dynamic Optimization.
- Meta Heuristics, Tabu Search, Genetic Algorithms and Hybrids.
- Parallel Processing, and Distributed Simulation.
- Embedded Systems (Hardware/Software Co-design).
- Real Time Operating Systems.

PROFESSIONAL EXPERIENCE:

• Teaching Experience:

Sep 15-	◇ VLSI Electronic Design Automation (Grad Course, ENG6600), UOG.
Jan 06-Jan 17	◇ Reconfigurable Computing Systems (Grad Course, ENG6530), UOG.
Jan 14-Jan 14	◇ Logic Synthesis (ENG3190), University of Guelph (UOG).
Jan 10-Jan 16	◇ Reconfigurable Computing Systems (Undergrad Course, ENG3050), UOG.
Sep 01-Sep 17	◇ Digital Design (ENG2410), University of Guelph (UOG).
Sep 99-Sep 13	◇ Microcomputer Interfacing (ENG3640), University of Guelph.
Jan 02-Jan 03	◇ VLSI Design (Grad Course, ENG6090), UOG.
Jan 00-Jan 03	◇ Optimization for Engineering (Grad Course, ENG6410), UOG.
Jan 01-May 01	◇ Network Theory (ENG2450), UOG.
May 99-May 00	◇ Circuit & Systems (GEN123), University of Waterloo.
Jan 98-Jan 99	◇ VLSI Design (ELE863), University of Ryerson.
Jan 98-Jan 99	◇ Real Time Operating Systems (ELC648), Ryerson University.

• Research Experience:

1999 - 2018 **Professor, University of Guelph, Guelph, Ontario**

- Research: Physical Design Automation, Reconfigurable Computing.
  The main objectives of this research are directed towards developing algorithmic solutions for VLSI CAD in general and circuit layout in particular. The research involves exploring the effectiveness of integrating exact mathematical methods based on linear/non-linear programming with efficient advanced search techniques in the form of Tabu Search, and Genetic Algorithms along with Machine Learning. The research is also targeted towards designing hardware platforms based on FPGAs in the form of accelerators to speedup the performance of Advanced Search Heuristics such as Genetic Algorithms and Tabu Search.

Aug 97 - 99 **Assistant Professor, Ryerson University, Toronto, Ontario**

- Research: Physical Design (Circuit Partitioning, Placement and Routing). VLSI Circuit Design and Real Time Operating Systems.

Jan 98 - 01 **Adjunct Professor, University of Waterloo, Waterloo, Ontario**

- Research: VLSI Circuit Layout Design (Design Automation Group)
  - Effective partitioning schemes for ASICs and FPGAs.
  - Placement and global routing schemes for standard cell design styles.
  - Integration of the above with an industry based tool i.e Cadence.

May 91 - 94 **Ph.D Candidate, University of Waterloo, Waterloo, Ontario**

The research involves exploring algorithmic solutions to the problem of circuit layout in VLSI design. The proposed research attempts to use advanced search methods in the form of Tabu Search, Genetic Algorithms and Neural Networks to successfully solve the combinatorial aspect in reasonable amount of time. An effective means to accomplish this is to dynamically tune parameters of

these algorithms to enhance their performance. A more important research avenue involved integrating these fundamentally different approaches as a means to avoid many of the weaknesses inherent in each methodology, while capitalizing on their strengths.

Jan 88 - 91 **M.A.S.c Candidate, University of Waterloo, Waterloo, Ontario**
Simulation of complex discrete event system are usual exceedingly slow and are notorious consumers of CPU cycles. Our important research goal was to speed up simulations by exploiting concurrency inherent in them. The research proposes a special purpose hardware accelerator for distributed discrete event simulation based on Time Warp mechanism. The main features of the architecture are the exploitation of logic circuit concurrency and algorithm concurrency. Simulations of the proposed architecture indicate that the accelerator demonstrate a performance improvement by a factor of 2 over a single CPU in terms of speed and reduction of roll-backs.

Dec 83 - 84 **BS.c Program, Tripoli University, Tripoli, Libya**
Design of a data acquisition system for sampling speech and algorithms for speech recognition. This system was capable of achieving a recognition of 100 phrases with 87% accuracy. Implementation was based on an Apple Computer with limited amount of memory (128 K) and most algorithms used for speech recognition were based on 6502 assembly language.

• Graduate Supervision:

1999 - 2018 **University of Guelph (Graduate Students)**

- Mr. M. Thompson, M.Sc., "A Clustering Utility Based Approach for ASIC Design", **Completed June 2000**
- Mrs. Z. Yang, M.Sc., "Area/Congestion-driven Placement for VLSI Circuit Layout", **Completed Aug 2003**
- Mrs. G. Koonar, M.Sc., "A Reconfigurable Hardware Implementation of Genetic Algorithms for VLSI CAD Design", **Completed Aug 2003**
- Mr. K. Nichols, M.Sc., "A Reconfigurable Computing Architecture for Implementing Artificial Neural Networks on FPGAs", **Completed Dec 2003**
- Mr. P. Du, M.Sc., "Fast Heuristic Techniques for FPGA Placement Based on Multilevel Clustering", **Completed Dec 2003**
- Mr. W. Wang, M.Sc., "Low Power Multi-Threshold CMOS Circuits Optimization and CAD Tool Design", **Completed May 2004**
- Mr. H. Sun, M.Sc., "Sequential/Parallel Global Routing Algorithms for VLSI Standard Cells", **Completed May 2004**
- Mr. X. Li, M.Sc., "A Hardware/Software Co-design for Artificial Neural Networks", **Completed Aug 2004**
- Mr. X. Bao, M.Sc., "Constructive/Iterative Based Heuristics for FPGA Placement", **Completed Aug 2004**

- Mr. S. Coe, M.Sc., "A Memetic Algorithm Implementation on a FPGA for VLSI Circuit Partitioning", **Completed Aug 2004**
- Mr. A. Shamli, M.Sc., "Optimization in Dynamic Environments for Robot Path Planning", **Completed Aug 2004**
- Mr. G. Lu, M.Sc., "Sequential/Parallel Heuristic Algorithms for VLSI Standard Cell Placement", **Completed Sep 2004**
- Mr. V. Pandya, M.Sc., "A Handel-C Implementation of the Back Propagation Algorithm on FPGAs", **Completed Oct 2005**
- Mr. F. Li, M.Sc., "A Hardware/Software Co-Design of the FM Partitioning Algorithm", **Completed Jan 2006**
- Mr. A. Savich., "Mapping Multiple Expert Systems (ANNs) on FPGAs", **Completed Sep 2006**
- Miss. C. Freeman., "Classification of Audio", **Completed Dec 2007**
- Mr. A. Sagir, M.Sc.., "Reconfigurable Architectures for WiMax", **Completed Aug 2008**
- Mrs. Z. Yang, Ph.D., "Global Routing Techniques for DSM VLSI Circuit Layout", **Completed May 2008**
- Mr. M. Ghazali, M.Sc.., "Hardware Accelerators for VLSI Global Routing", **Completed April 2009**
- Mr. J. Huissman, M.Sc.., "Scheduling for Multi-Processor Systems", **Completed May 2009**
- Mr. D. Hermann, M.Sc.., "DSP Algorithms for Hearing Aids", **Completed May 2009**
- Mr. A. Elhossini, Ph.D., "Reconfigurable Computing for DSP Systems", **Completed Dec 2009**
- Mrs. S. Shiek, M.Sc., "Sequential Classification for Medical Data", **Completed Aug 2012**
- Mr. O. Ahmed, Ph.D., "Reconfigurable Architectures for Packet Classification", **Completed July 2013**
- Miss. L. Richards, M.Sc., "Classification Algorithms for Record Linkage", **Completed Aug 2013**
- Mr. G. Lacey, M.Sc., "Acceleration for Deep Learning", **Completed Aug 2016**
- Mr. R. Pattison, M.Sc., "Advanced EDA Tools for FPGAs", **Completed Aug 2015**
- Mr. A. Al-wattar, Ph.D., "Operating Systems for RTR Architectures", **Completed in Apr 2015**
- Mrs. D. Jamma, M.Sc.., "Hardware Accelerators for Machine Learning", **Completed in May 2016**
- Mr. Z. Abouwaimer, Ph.D., "Efficient CAD Tools for FPGA Placement", **To be completed in April 2018**
- Mr. A. Shamli, Ph.D., "Data Mining for Hyperspectral Images", **To be completed in Dec 2019**
- Mrs. A. Alhyari, Ph.D., "Optimal Sequence Design for FPGA CAD Flow", **To be completed August 2019**

- Mr. T. Martins, MSc., "Congestion Estimation for FPGAs",
  To be completed Dec 2019
- Mr. M. Sharma, M.ENG., "Machine Learning for Embedded Applications",
  To be completed Sept. 2019
- Mr. R. Mital, M.ENG., "Machine Vision for Embedded Applications",
  To be completed Dec. 2019

• URA/USRA, Undergraduate Supervision:

1999 - 2018 **University of Guelph, (Undergraduate Research Assistants)**

- D. Noel, "Implementation of B2B for FPGA Placement", May-Aug 2019
- J. Foxcroft, "Congestion Estimation for FPGA Placement", May-Aug 2019
- T. Martin, "Algorithms for FPGA Packing", May-Aug 2017
- J. Fox, "Algorithms for FPGA Placement", May-Aug 2017
- D. Marouf, "Algorithms for FPGA Routing", May-Aug 2017/2018
- A. Gunter, "Machine Learning for Electronic Design Automation", May-Aug 2017
- R. Pazhekattu, "Vision on Reconfigurable Computing Systems", May-Aug 2015
- K. Ali, "Using WEKA for Machine Learning Applications", May-Aug 2015
- A. Ahmed, "Optimization of Wireless Sensor Networks", May-Aug 2014
- J. Winer, "Operating System Support for Reconfigurable Systems", May-Aug 2013
- A. Agrawl, "Support Vector Machines for Data Mining Systems", May-Aug 2011
- A. Erb, "Hardware Accelerators for Data Mining Systems", May-Aug 2011
- K. Chata, "Hardware Accelerators for Packet Classification", May-Aug 2010
- B. Debowski, "Scheduling Algorithms for Embedded Systems", May-Aug 2009
- J. Beukert, "Parallel Based Algorithms for Path Planning", May-Aug 2004
- A. Savich, "Generic VHDL Implementation of ANNs", May 2004
- C. Lemieux, "Reconfigurable Computing Systems", May 2004
- M. Walia, "Preprocessing Techniques for Circuit Layout", May 2003
- L. St Onge, "Hardware/Software Co-design Automation", May 2001
- H. Homayounfar, "Electronic Tutor", May 2001
- K. Desroucher, "Reconfigurable Computing", May 2000
- M. Bakhbakhi, "GUI for Circuit Placement", Jan 2000
- M. Xie, "New Techniques for Circuit Partitioning", May 1998

• 4th Year Design Projects:

1999 - 2018 **University of Guelph, (4th Year Design Projects)**

- L. Spivak, "Muscular Contraction Safety Interface", Jan-Apr 2017
- T. Clay, "Heat Illness Monitoring System", Jan-Apr 2017
- A. Zepeda, "Autonmous Personal Assistant", Sep-Dec 2015
- M. Pawlak, "Automated Gloss Meter Reading and Recording", Sep-Dec 2012
- J. Gibbs, "Self Sustaining Heated Driveway", Sep-Dec 2012

- B. Lahartinger, "Wireless Home Automation Control", Jan-Apr 2010
- T. Ludikar, "Intelligent Autonomous Aerial Rescue Platform", Jan-Apr 2009
- P. Walker, "High Definition Adapter for the CanTrans", Jan-Apr 2009
- C. Miculescu, "Design of a Wireless 5.1 Digital Surround System", Sep-Dec 2009
- B. Debowski, "Dynamic Path Planning", Sep-Dec 2008
- K. Butler, "A DSP Communication System in a Factory Setup", Jan-Apr 2008
- E. Love, "Local Positioning System", Jan-Apr 2008
- J. Hilliard, "Image Processing for Fingerprint Authentication", Jan-Apr 2007
- D Ifrim, "A Construction Bypass Traffic Routing Systems", Sep-Dec 2007
- C. Lemieux, "Wireless Systems for Accident Avoidance", Jan-Apr 2006
- P. Patel, "Speech Recognition to Assist the Disabled", Jan-Apr 2006
- K. Sinitksi, "Finger Print Based User Authentication", Sep-Dec 2005
- J. Hones, "Team Gryphon Robot Soccer", Jan-Apr 2005
- S. Bradey, "Electro-Pneumatic Shifting System", Jan-Apr 2005
- G. Nasby & J. Wood, "Control Systems for RoboSoccer", Jan-Apr 2004
- R. Armstrong & R. Clubbe, "A Vision System for RoboSoccer", Jan-Apr 2004
- D. Cibic & P. Koller, "The S.E.A.N Robot", Jan-Apr 2003
- P. Parkitny & J. Goertz, "Fuel Injection System, RTX", Jan-Apr 2003
- R. Battiston & T. Hamm, "Robot Navigation Systems", Jan-Apr 2003
- R. Danford & P. Wighton, "Power-line Communications", Jan-Apr 2003
- G. Callow & P. Okeefe, "High Speed PCI on FPGA", Sep-Dec 2002
- T. Wu & D. Rule, "Ethernet Tap Device", Jan-Apr 2002
- G. Knapp & C. Peart, "USB Based Data Logger", Jan-Apr 2002
- R. Meyenburg & B. Millen, "Object Tracking", Jan-Apr 2002
- M. Kay & M. Sewell, "Parking Lot Communication", Jan-Apr 2002
- V. Haramina & S. Kulas, "Voice Controlled Robot", Sep-Dec 2001
- C. Church & M. Minogue, "Multi Agent Systems", Jan-Apr 2001

• Industrial Experience:

Apr 95 - Aug 97 **Shell Research BV, Amsterdam**.
Research Mathematician:
- Enhanced the performance of a Vehicle Routing and Scheduling package (CROSS) at Shell International Oil Products.
- Developed an auto-routing engine for Shell Company (CROSS) vehicle routing and scheduling package based on digitized maps.
- Redesigned a new engine for CROSS vehicle routing and scheduling package based on a Column Generation Technique.
- Enhanced the performance of a Secondary Distribution Package (Synopsys).

Oct 86 - Aug 87 **Areson Import Export Company, Rabat Morroco**.
Software Engineer:
- Supervised the installation of a computer system.
- Responsible for writing payroll programs for the company.
- Trained personnel in support of products.

Dec 85 - Sep 86 **AES Company, Tripoli Libya**.

Computer Engineer:
- Developed an interface to debug the 7100 AES cluster system.
- Modified several boards for the disk controller.
- Updated the ROM diagnostic for the daisy wheel printer.
- Analyzed system failure causes on customer sites.

Jul 84 - Nov 85 **NCR Company, Tripoli Libya**.
Computer Engineer:
- Investigated failure causes of NCR 9010 system and modified boards.
- Trained personnel in H/W fault diagnosis for the NCR 9010 system.
- Supervised the installation of several computer sites.
- Discussed the needs of banking systems and developed accounting programs.

• Consulting and Industrial Contacts:

Aug 17 **Advanced Micro Devices (AMD), Toronto**
- Development and Mapping of Cryptographic Algorithms onto Field Programmable Gate Arrays.

Dec 14 **Magnum Semiconductor, Waterloo**
- Development and Mapping of Video Compression Algorithms onto Field Programmable Gate Arrays.

Jun 11 **ResourceH2O, Guelph**
- Smart Panel for ResourceH2O Rainwater Harvesting

Aug 05 **PolarSat, Montreal**
- Adapting WiMax for Satellite Communication Systems

June 02 **AMIS Inc., Waterloo**
- NSERC Collaborative Grant to support several graduate students to design and map noise cancellation algorithms on FPGAs.

May 00 **Sequence Design Automation, San Jose**
- Contacts with Sequence Design Automation (previously Sapphire Design) were established at the Design Automation Conference in June 2000. Agreement to Collaborate on several projects including Global Routing and Performance Driven Placement.

Jan 99 **Intel & Texas Instruments**
- Initial contacts with VLSI companies such as Intel Corporation and Texas Instruments have been made to test the developed CAD tools on their designs and achieve further support in the near future.

Dec 98 **Shell Research BV, Amsterdam**
- Investigating further optimization techniques for Shell International Oil Products in the Hague for their "Vehicle Routing and Scheduling ". Systems".

Sep 98 **Nortel, Ottawa**
- Collaboration with Professor K. Ponnambalam in the "Systems Design Department at the University of Waterloo". As part of the research project with NORTEL, we are developing new multi-objective optimization techniques for high-level design of large-scale software structures in

telecommunication systems. The techniques use various software metrics suitable for structured and object-oriented design.

SERVICE & ADMINISTRATION:

School of Engineering

- Program Leader for Computer Engineering Program, 2012 - 2015.
- Member, Curriculum Committee, 2012 - 2014.
- Member, Promotion and Tenure Committee, 2012 - 2014.
- Member, Pathway Program Committee, 2010 - 2011.
- Member, Graduate Committee, 2006 - 2018.
- Member, Program Committee, 2007 - 2018.
- Member, Computer Committee, 2009 - 2010.
- Member, Work Load Committee, 2009 - 2010.
- Member, Planning Committee, 2009.
- Chair, Space Committee, 2007 - 2009.
- Chair, Computer Committee, 2006 - 2008.
- Member, Search Committee for Electronics Technician, 2006, 2008.
- Member, Search Committee for Lab Instructor, 2014, 2017.
- Member, Awards Committee, 2003.

University of Guelph

- Member of Liaison Committee, department of computing and information Science, 2010.
- Member, University of Guelph UGFA Teaching Award Committee, 2009.
- Member, University of Guelph Senate, 2007-2009.

University of Ryerson, ECE Dept

- Member, Hiring Committee, new faculty member, 1998.
- Member, Computer Committee, 1997.
- Liaison and Rep of Canadian Microelectronics Corporation, 1999.

External: Academic

- External Examiner for PhD Exams, Jan 2010, Jan 2015.
- Member, Georgia National Sci Foundation, GNSF, 2009-2010.
- Member of OGS Panel, Ministry of Training, 2008
- Member of NSERC CRD Grant Application, 2007
- Reviewer for NSERC Discovery Grant Applications, 2006
- Reviewer for NSERC Strategic Projects, 2004

- Member of NSERC Grant Selection Committee, 2004
- Member, MOTEX Multi-disciplinary Optimizatin for Design Excellence, 2002-2004.

External: Professional

- Professional Engineer Monitor, Second Foundation Consulting.
- Professional Engineer Ontario, Examiner (Report Marking).
- Liaison for Canadian Microelectronics Corporation, Kingston, Ontario.
- IEEE Student branch counselor for the University of Guelph.
- Technical advisory committee member for "PolarSat Inc", Montreal, Canada.
- Technical advisory board for "Sequence Design Automation", San Jose, California.

External: Technical

- Associate Editor of ISCA Journal of Computers and Applications, 2005-2007.
- Member, Technical Program Committee, ReConFig Conference, 2006-2010.
- Member, Technical Program Committee, ICM Conference, 2008-2010.
- Member, Technical Program Committee, GECCO Conference, 2007-2009.
- Member, Technical Program Committee, IASTED Conference, 2008-2009.
- Invited Session organizer for CORS, INFORMS, 2004

PROFESSIONAL AFFILIATIONS:

IEEE	Institute of Electrical and Electronics Engineers.
ACM	Association for Computing Machinery.
ISCA	International Society for Computer Applications.
PEO	Member & License holder, Professional Engineers of Ontario.
SDA	Sequence Design Automation (San Jose, CA).
CMC	Canadian Micro-electronic Corporation.
MMO	Materials and Manufacturing Ontario.
CITO	Communication and Information Technology Ontario.
DAG	Design Automation Group at University of Waterloo.
ISGEC	International Society For Genetic and Evolutionary Computation.
SIAM	Society of Industrial and Applied Mathematics.

PATENTS:

24. Jan. 2012	Co-inventor of "Architecture, System and Method for ANN Implementation I" Patent Number: 8103606, Filed 10/12/2007, Issued **24/01/2012**.
18. June 2013	Co-inventor of "Architecture, System and Method for ANN Implementation II" Patent Number: 8468109, Filed 28/12/2011, Issued **18/06/2013**.

AWARDS, SCHOLARSHIPS:

Aug. 19	Best paper Award in 29th International Conference on FPL, 2019.
Dec. 18	Best paper Award in International Conference on Microelectronics, 2018.
Aug. 18	Best paper Award in 28th International Conference on FPL, 2018.
May. 17	Best paper Award in 24th Reconfigurable Architecture Workshop, 2017.
Oct. 16	Best paper Award in IEEE System and Tech. for Remote Sensing Applications, 2016.
Apr. 16	3rd Place in ISPD Routing-Driven FPGA Placement Contest, 2016.
Apr. 12	Elevated to IEEE Senior Member grade, 2012.
May. 09	Best paper in IEEE Canadian Conference on ECE, 2009.
Oct. 08	Distinguished Professor Teaching Award, 2008.
Jun. 07	Best paper in IEEE Symposium on Signal Processing, 2007.
Jul. 01	Best paper in 5th World Multi Conference SCI 2001.
Jan. 92 - May 93	University of Waterloo Graduate Scholarships.
May. 90 - Jan 91	Ontario Graduate Scholarship, OGS.
Sep. 89 - Jan 90	University of Waterloo Graduate Scholarships.
Jan. 79 - May 84	Al-Fateh University Scholarship.

RESEARCH GRANTS:

Sep. 17 -Feb 18	NSERC Engage, 30,000$. "Design Exploration of Cryptographic Accelerators".
Apr. 17 -Apr 22	NSERC Discovery, 140,000$. "FPGA Electronic Design Automation".
Aug. 16 -Aug 17	Huawei Technologies, Co-Principal Inv., 123,841$. "Machine Learning Hardware Acceleration".
Jul. 14 -Dec 14	NSERC Engage, 30,000$. "Hardware Accelerators for Video Compression".
May. 11 -Dec 11	OCE Technical Problem Solving Light, 50,000$. "A Smart Panel for Rainwater Harvester".
Mar. 12 -Mar 17	NSERC Discovery Grant, 90,000$. "Design Exploration for Dynamic Runtime Reconfigurable Architectures".
Sep. 07 -Mar 12	NSERC Discovery Grant, 90,000$. "A Unified Congestion Driven Power Aware Methodology for VLSI Physical Design Automation".
Sep. 07 -Sep 09	OCE Market Readiness, 131,000$. "Development of an Advanced Neural Processor for Data Mining Applications".
Sep. 04 -Sep 07	NSERC, CRD 140,000$. "Intelligent Noise Reduction for Acoustic Signal Processing: A Hardware-Software Co-design Approach".
Jan. 04 -Dec 06	MMO Collaborative, 271,200$. "Real-time Shop-floor Scheduling for Cooperative Distributed Manufacturing".

Apr. 02 -May 06	NSERC Discovery Grant, 100,000$. "A Distributed Adaptive Hardware/Software CAD Methodology for VLSI System on a Chip".
Sep. 02 -Sep 04	Sharcnet Graduate Fellowship, 44,000$. "Distributed Advanced Search Techniques and Meta-heuristics for VLSI Computer Aided Design".
Aug. 99	School of Engineering Startup Grant, 25,000$.
Apr. 98 -May 02	NSERC Discovery Grant, 68,000$. "VLSI Physical Design Automation".
Nov. 97	Applied Science Research Starter Grant, 5,000$.

PUBLICATIONS, PRESENTATIONS:

Book Chapter (Published/Accepted)

[1] A. Younes and S. Areibi and P. Chalami and O. Basir. "Adapting Genetic Algorithms for Combinatorial Optimization Problems in Dynamic Environments". *Book Chapter on Evolutionary Computations*, **Fall 2008**.

[2] A. Younes and A. Elkamel and S. Areibi. "Genetic Algorithms in Chemical Engineering: A Tutorial". *Book Chapter on Evolutionary Computations in Chemical Engineering*, **Fall 2008**.

[3] A. Younes and A. Elkamel and S. Areibi. "Meta-heuristics: Evaluation and Reporting Techniques". *Book Chapter on Evolutionary Computations in Chemical Engineering*, **Fall 2008**.

[4] M. Moussa and S. Areibi and K. Nichols. "On the Arithmetic Precision for implementing Back-propagation networks on FPGAs: A Case Study". *Book Chapter on FPGA Implementation of Neural Networks*, pp:37-61, **Fall 2006**.

[5] S. Areibi. "Effective Exploration and Exploitation of the Solution Space via Memetic Algorithms". *Book Chapter on Recent Advances in Memetic Algorithms and Related Search Technologies*, pp:161-182, **Fall 2005**.

Journals (Published/Accepted)

[1] A. Alhyari and Z. Abouwaimer and G. Grewal and S. Areibi and T. Martin and D. Maarouf and A. Vannelli "ACM Transactions on Reconfigurable Technology and Systems (TRETS)". *Novel Congestion Estimation and Routability-Prediction Methods based on Machine Learning for Modern FPGAs*, **September 2019**.

[2] Z. Abouwaimer and D. Maarouf and T. Martin and J. Foxcroft and G. Grewal and S. Areibi and A. Vannelli "ACM Transactions on Design Automation of Electronic Systems (TODAES)". *GPlace3.0: Routability-Driven Analytic Placer for UltraScale FPGA Architectures*, **August 2018**.

[3] A. Al-Hyari and S. Areibi "Journal of Computational Vision and Imaging Systems". *Design Space Exploration of Convolutional Neural Networks based on Evolutionary Algorithms*, **October 2017**.

[4] A. Elshamli and G. Taylor and A. Berg and S. Areibi "IEEE Journal Selected Topics in Applied Earth Observations and Remote Sensing". *Domain Adaptation Using Representation Learning for the Classification of Remote Sensing Images*, **June 2017**.

[5] A. Al-Wattar and S. Areibi and G. Grewal "An Efficient Evolutionary Task Scheduling/Binding Framework for Reconfigurable Systems". *Journal of Reconfigurable Computing*, **March 2016**.

[6] A. Al-Wattar and S. Areibi and G. Grewal "An Efficient Framework for Floorplan Prediction of Dynamic Runtime Reconfigurable Systems". *International Journal of Reconfigurable and Embedded Systems*, **July 2015**.

[7] R. Collier and C. Fobel and R. Pattison and G. Grewal and S. Areibi "Advancing Genetic Algorithm Approaches to FPGA Placement with Enhanced Recombination Operators". *Journal of Evolutionary Intelligence*, **Oct. 2014**.

[8] A. Savich and S. Areibi "A Low Power Scalable Stream Compute-Accelerator for General Matrix Multiplication". *Journal of VLSI Design*, **Dec. 2013**.

[9] A. Elhossini and S. Areibi and R. Dony "An Architecture Exploration Framework for The Implementation of Embedded DSP Applications". *Journal of VLSI Design*, **August. 2013**.

[10] O. Ahmed, S. Areibi and R. Collier and G. Grewal "An Impulse-C Hardware Accelerator for Packet Classification Based on Fine/Coarse Grain Optimization". *Journal of Reconfigurable Computing*, **July 2013**.

[11] O. Ahmed, S. Areibi and G. Grewal "Hardware Accelerators Targeting a Novel Group Based Packet Classification Algorithm". *Journal of Reconfigurable Computing*, **Feb. 2013**.

[12] M. Walton, G. Grewal, O. Ahmed and S. Areibi "An Empirical Investigation on System Statement Level Parallelism for Accelerating Scatter Search using Handel-C and Impulse-C". *VLSI Design*, **July 2012**.

[13] O. Ahmed, K. Chattha, S. Areibi and B. Kelly "PCIU: Hardware Implementation of an Efficient Packet Classification Algorithm with an Incremental Update Capability". *Hindawi, International Journal of Reconfigurable Computing*, **July 2011**.

[14] A. Savich, M. Moussa and S. Areibi. "A Scalable Pipelined Architecture for Real-Time Computation of MLP-BP Neural Networks". *Microprocessors and Microsystems*, In Press **March 2011**.

[15] M. Xu, G. Grewal, S. Areibi, C. Obimbo and D. Banerji "StarPlace: An Efficient and Effective Analytic Method for FPGA Placement". *Elsevier, Integration, The VLSI Journal*, V: 44, No: 3, pp: 192-204 **June 2011**.

[16] M. Xu, G. Grewal, S. Areibi, C. Obimbo and D. Banerji. "Near Linear Wirelength Estimation for FPGA Placement". *Canadian Journal of Electrical and Computer Engineering*, V: 34, No: 3, Pages: 125-132, **Summer 2010**.

[17] A. Elhossini, S. Areibi and R. Dony. "Strength Pareto Particle Swarm Optimization and Hybrid EA-PSO for Multi-Objective Optimization". *Evolutionary Computation Journal*, V: 18, No: 1, Pages: 127-156, **Spring 2010**.

[18] A. Nour, Z. Yang, M. Anis, S. Areibi, A. Vannelli and M. Elmasry. "A Power Efficient Multi-Pin ILP Based Routing Technique". *IEEE Transactions on Systems and Circuits*, V: 57, No: 1, Pages: 225-235, **January 2010**.

[19] A. Sagier, S. Areibi and R. Dony. "Implementation Approaches Trade-offs for WiMax OFDM Functions on Reconfigurable Platforms". *ACM Transactions on Reconfigurable Technology and Systems*, V: 3, No: 3, Pages:1-28, **September 2010**.

[20] L. Rakai and L. Behjat and S. Areibi and T. Terlaky. "A Multi-level Congestion Based Global Router", *Journal of VLSI*, V: 2009, No: 6, Pages: 1-13, **September 2009**.

[21] S. Areibi, X. Bao, G. Grewal, D. Banerji and P. Du. "A Comparison of Heuristics for FPGA Placement". *ACTA International Journal of Computers and Applications*, Vol. 16, No. 1, pp:13-33, **March 2009**.

[22] C. Freeman, R. Dony and S. Areibi. "A Comparison of Classification Techniques for Audio Environment Classification". *Int. Journal of Information Technology and Intelligent Computing*, Vol. 2, No. 3, pp: xxxx, **June 2007**.

[23] Z. Yang, S. Areibi, and A. Vannelli. "An ILP Based Hierarchical Global Routing Approach for VLSI ASIC Design". *Journal of Optimization Letters*, Vol.1, No. 3, pp:281-297, **June 2007**.

[24] S. Coe, S. Areibi and M. Moussa. "A Hardware Memetic Accelerator for VLSI Circuit Partitioning". *International Journal of Computers and Applications*, Vol. 33, pp:233-248, **May 2007**.

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